UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,901	08/16/2000	Subramania Sudharsanan	P-2616	3352

24209 7590 11/26/2008

GUNNISON MCKAY & HODGSON, LLP
1900 GARDEN ROAD
SUITE 220
MONTEREY, CA 93940

EXAMINER	
UNELUS, ERNEST	
ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
11/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/640,901	SUDHARSANAN ET AL.	
	Examiner	Art Unit	
	ERNEST UNELUS	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,18,20-27,33,35-40 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43* is/are allowed.

6)☒ Claim(s) *1,2,4,18,20-22,33 and 35-40* is/are rejected.

7)☒ Claim(s) *23-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

Applicant's arguments filed 07/07/2008 with respect to claims 1, 2, 4, 18, 20-27, 33, 35-40, and 43 have been fully considered but are moot in view of the new ground(s) of rejection.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

The applicant's drawings submitted are acceptable for examination purposes.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section

> 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 27 is rejected under 35 U.S.C. 102(e) as being anticipated by Kanakogi et al., U.S. Patent Number 6,609,143 (herein referred to as Kanakogi).

2. Referring to claim 27, Kanakogi has taught a computer program product encoded on one or more machine-readable media, the computer program product comprising:

a. an instruction sequence, the instruction sequence including an instance of a parallel multiply add instruction (Kanakogi column 1 lines 24-61 figure 12);

b. the instance of the parallel multiply add instruction having an at least four operand instruction format, wherein execution of the parallel multiply add instruction causes generation of a first product from a first operand's first component and a second operand's first component, in parallel with generation of a second product from the first operand's second component and the second operand's second component, causes generation of a first sum from the first product and a third operand's first component, in parallel with generation of a second sum from the second product and the third operand's second component, and causes the first sum to be stored in accordance with a fourth operand's first component and the second sum to be stored in accordance with the fourth operand's second component (Kanakogi column 1 lines 24-61 figure 12).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 18, 20, 21, and 33-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanakogi et al., U.S. Patent Number 6,609,143 (herein referred to as Kanakogi) in view of Imamura, U.S. Patent Number 6,725,355 (herein referred to as Imamura).

5. Referring to claim 1, Kanakogi has taught a method of executing a single instruction parallel multiply-add function on a processor, the method comprising:

a. providing the processor with an opcode indicating a parallel multiply-add instruction having an operand;

providing the processor with a first, a second and a third value, wherein each of the values comprises two or more operand components (Kanakogi column 1 lines 24-61 figure 12);

b. multiplying first operand components of the first and the second values to generate a first intermediate value; multiplying second operand components of the first and the second values to generate a second intermediate value; adding a first operand component of the third value to the first intermediate value to generate a first result value (Kanakogi column 1 lines 24-61 figure 12);

c. adding a second operand component of the third value to the second intermediate value to generate a second result value; storing the first result value in a first portion of a result location; and storing the second result value in a second portion of the result location (Kanakogi column 1 lines 24-61 figure 12).

but fails to disclose expressly providing the processor with a first, a second and a third value of a first operand, a second operand and a third operand, respectively in said at least three operands.

Imamura discloses providing the processor with a first, a second and a third value of a first operand, a second operand and a third operand, respectively in said at least three operands (Imamura column 16 lines 22-27).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a processor with multiple values having three operands, as taught by Oberman and Imamura, in the processor of Kanakogi, to arrive at the claimed conditional pick instruction, for the desirable purpose of speeding up the execution of a program in the processor.

6. Referring to claim 2, Kanakogi has taught the method of claim 1, as described above, and wherein the first, second and third values are stored in respective source registers of the processor specified by the parallel multiply-add instruction, and the first and the second result values are stored in a destination register of the processor specified by the parallel multiply-add instruction (Kanakogi column 1 lines 24-61 figure 12).

7. Referring to claim 4, Kanakogi has taught the method of claim 1, as described above, and wherein the processor is pipelined and the single instruction is executed with a throughput of one

instruction every 2 cycles (Kanakogi column 1 lines 24-61 figure 12; since there is a register in the process, two clock signals would have to be completed before the results were stored).

8. Referring to claim 18, Kanakoi has taught a processor comprising:

a. a first and second multiplier paths (Kanakogi figure 12 elements 101 and 102)

b. a first and second adder paths (Kanakogi figure 12 elements 103and 104)

c. and wherein the processor supports a parallel multiply-add instruction, the parallel multiply add instruction having an operand executable to cause the processor to, in parallel, route a first component of a first operand and a first component of a second operand to the first multiplier path and a second component of the first operand and a second component of the second operand to the second multiplier path, in parallel, route output of the first multiplier path and a first component of a third operand to the first adder path, and output of the second multiplier path and a second component of the third operand to the second adder path, and store output of the first adder path at a first location and output of the second adder path at a second location (Kanakogi column 1 lines 24-61 figure 12).

but fails to disclose expressly providing the processor with instruction having a least three operands.

Imamura discloses providing the processor with instruction having a least three operands (Imamura column 16 lines 22-27).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a processor with multiple values having three operands, as taught by Oberman and Imamura, in the processor of Kanakogi, to arrive at the claimed conditional pick instruction, for the desirable purpose of speeding up the execution of a program in the processor

9. Referring to claim 20, Kanakogi has taught the processor of claim 19 (Claim 19 has been cancelled. It is improper for a claim to depend from a cancelled claim. So for the purposes of examination Examiner assumes that claim 20 is dependent on claim 18.), as described above, and wherein the results of the parallel multiply-add instruction are saturated (Kanakogi column 6 lines 38-46, figure 2; the extender makes sure thevalues are extended, or saturated).

10. Referring to claim 21, Kanakogi has taught the processor of claim 19, (Claim 19 has been cancelled. It is improper for a claim to depend from a cancelled claim. So for the purposes of examination Examiner assumes that claim 21 is dependent on claim 18.), as described above, and wherein the processor provides multiple saturation modes (Kanakogi column 6 lines 38-46, figure 2; the extender makes sure the values are extended, or saturated).

11. Referring to claim 27, Kanakogi has taught a computer program product encoded on one or more machine-readable media, the computer program product comprising:

a. an instruction sequence, the instruction sequence including an instance of a parallel multiply add instruction (Kanakogi column 1 lines 24-61 figure 12);

b. the instance of the parallel multiply add instruction having an at least four operand instruction format, wherein execution of the parallel multiply add instruction causes generation of a first product from a first operand's first component and a second operand's first component, in parallel with generation of a second product from the first operand's second component and the second operand's second component, causes generation of a first sum from the first product and a third operand's first component, in parallel with generation of a second sum from the second product and the third operand's second component, and causes the first sum to be stored in accordance with a fourth operand's first component and the second sum to be stored in

accordance with the fourth operand's second component (Kanakogi column 1 lines 24-61 figure 12).

12. Referring to claim 33, Kanakogi has taught a method of executing an instruction instance comprising: generating a first product and a second product in parallel, wherein the first product is from a first value in a first portion and a second value in a first portion and the second product is from a third value in a second portion and a fourth value in a second portion; and generating a first sum and a second sum in parallel, wherein the first sum is from the first product and a fifth value and the second sum is from the second product and a sixth value (Kanakogi column 1 lines 24-61 figure 12).
but fails to disclose expressly providing the processor with first, second, and third values in a first, second, and third portions of three operands instruction.

Imamura discloses providing the processor with first, second, and third values in a first, second, and third portions of three operands instruction (Imamura column 16 lines 22-27).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a processor with multiple values having three operands, as taught by Oberman and Imamura, in the processor of Kanakogi, to arrive at the claimed conditional pick instruction, for the desirable purpose of speeding up the execution of a program in the processor

13. Referring to claim 34, Kanakogi has taught the method of claim 33, as described above, and wherein the first and third values respectively are first and second portions of a first operand, the second and fourth values respectively are first and second portions of a second operand, and

the fifth and sixth values respectively are first and second portions of a third operand (Kanakogi column 1 lines 24-61 figure 12).

14. Referring to claim 35, Kanakogi has taught the method of claim 33, as described above, and further comprising storing, in parallel, the first sum in a first location and the second sum in a second location (Kanakogi column 1 lines 24-61 figure 12).

15. Referring to claim 36, Kanakogi has taught the method of claim 35, as described above, and wherein the first location is a first portion of a destination register and the second location is a second portion of the destination register (Kanakogi column 1 lines 24-61 figure 12).

16. Referring to claim 37, Kanakogi has taught the method of claim 33, as described above, and wherein the instruction instance is executed by a pipelined processor that performs operations for the instruction instance in 2 cycles (Kanakogi column 1 lines 24-61 figure 12; since there is a register in the process, two clock signals would have to be completed before the results were stored).

17. Referring to claim 38, Kanakogi has taught the method of claim 33, as described above, embodied as a computer program product encoded in one or more machine-readable media (Kanakogi column 1 lines 24-61 figure 12).

18. Referring to claim 39, Kanakogi has taught the processor of claim 18, as described above, and wherein the first store location is a first part of a register and the second store location is a second part of the register (Kanakogi column 1 lines 24-61 figure 12).

19. Referring to claim 40, Kanakogi has taught the process or of claim 18, as described above, and wherein the first store location is a first register and the second store location is a

second register (Kanakogi column 1 lines 24-61 figure 12; the results are split into a high register portion and a low register portion, which act as two separate registers).

20. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanakogi and Imamura, as applied to claim 1, and further in view of Oberman U.S. Patent Number 6,490,607 (herein referred to as Oberman) and Hennessy.

Referring to claim 22, Kanakogi has taught the processor of claim 18, as described above. Kanakogi has not taught wherein the processor further supports a conditional pick instruction, the conditional pick instruction executable to cause the processor to compare a first value to zero and to copy either a second value or a third value to a destination location depending on the comparison. Oberman has taught wherein the processor further supports a conditional pick instruction, the conditional pick instruction executable to cause the processor to compare a first value to zero and to copy either a second value or a third value to a destination location depending on the comparison (Oberman figure 14 column 6 lines 3-Since Oberman employs branching in its system, it would have been obvious to include the Branch if not equal to zero instruction, as taught by Hennessy, where the system compares a given value to zero, and then either branches to another place in the program, or continues on in order, depending on the result. These two scenarios will alter which value is then placed in the PC register.) (See Hennessy, pages 102 and 103 for the branch not equal to zero instruction.). The use of branching, and branch prediction using the branch if not equal to zero instruction speeds up the execution of a program by predicting whether the branch will change the next instruction to be processed or not. It would have been obvious to one of ordinary skill in the art at the time of the invention to use branching and branch prediction, as taught by Oberman and Hennessy, in the processor of

Kanakogi, to arrive at the claimed conditional pick instruction, for the desirable purpose of speeding up the execution of a program in the processor.

Allowable Subject Matter

21. Claims 23-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. Claim 43 is allowed.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

23. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

24. Per the instant office action, claims 1, 2, 4, 18, 20-27, and 33, 35-40 have received a final action on the merits.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

26. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 24, 20088

Ernest Unelus
Examiner
Art Unit 2181

/E. U./
Examiner, Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181